CLAIMS

What is claimed is:

1. A method for reducing the contact resistance of metal silicide contacts comprising the steps of:

(a) forming a metal germanium alloy layer over a silicon-containing substrate, wherein said metal is Co, Ti, Ni or mixtures thereof;

(b) annealing said metal germanium alloy layer at a temperature sufficient to convert at least a portion of said metal germanium alloy layer into a metal silicide layer that is substantially non-etchable compared to the unreacted metal germanium alloy layer, while forming a Si-Ge interlayer between said silicon-containing substrate and said substantially non-etchable metal silicide layer;

(c) removing any remaining metal germanium alloy layer, with the proviso that when Ti or Co are employed a second annealing step follows step (c) that is capable of converting the substantially non-etchable Ti or Co silicide phase into Co disilicide or C54 phase of $TiSi_2$.

2. The method of Claim 1 further comprising pre-annealing the metal germanium alloy layer prior

to step (b) at a temperature sufficient to form a metal rich germanium silicide layer.

3. The method of Claim 1 wherein said metal germanium alloy layer is formed by a deposition process selected from the group consisting of - chemical vapor deposition (CVD), plasma-assisted CVD, sputtering and evaporation, or said metal germanium alloy layer is formed by first depositing said metal to form a metal layer and then doping said metal layer with germanium.

4. The method of Claim 1 further comprising forming an optional barrier layer over said metal germanium alloy layer prior to step (b), wherein said optional barrier layer is removed by step (c).

5. The method of Claim 1 wherein said metal germanium alloy layer further includes at least one additive selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

6. The method of Claim 5 wherein said additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt or mixtures thereof

7. The method of Claim 6 wherein said additive is Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or mixtures thereof.

8. The method of Claim 1 wherein said metal germanium alloy layer contains from about 0.01 to about 50 atomic % Ge.

9. The method of Claim 8 wherein said metal germanium alloy layer contains from about 0.1 to about 20 atomic % Ge.

10. The method of Claim 1 wherein said metal of said metal germanium alloy layer is Co.

11. The method of Claim 4 wherein said optional oxygen barrier layer is composed of TiN.

12. The method of Claim 1 wherein said silicon-containing substrate comprises a single crystal Si, polycrystalline Si, SiGe, amorphous Si, or a silicon-on-insulator (SOI).

13. The method of Claim 2 wherein said pre-annealing step is carried out using rapid thermal annealing (RTA).

14. The method of Claim 13 wherein said RTA is carried out at a temperature of from about 350° to about 450°C for a time period of about 300 seconds or less

15. The method of Claim 1 wherein said annealing step (b) is carried out by RTA.

16. The method of Claim 15 wherein said RTA is carried out at a temperature of from about 400° to about 700°C for a time period of about 300 seconds or less.

17. The method of Claim 1 wherein said remaining metal germanium alloy layer is removed utilizing a wet etch step that includes the use of an etchant that is selective for removing said layer.

18. The method of Claim 1 wherein said second annealing step is carried out by RTA.

19. The method of Claim 18 wherein said RTA is carried out at a temperature of from about 700° to about 900°C for a time period of about 300 seconds or less.

20. The method of Claim 1 wherein said metal is Ni and Ni monosilicide is formed after step (b).

21. The method of Claim 1 wherein said metal is Co and Co monosilicide is formed after step (b).

22. The method of Claim 1 wherein said metal is Ti and C49 phase of $TiSi_2$ is formed after step (b).

23. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said substrate and said first layer are separated by a Si-Ge interlayer.

24. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of Ni monosilicide, wherein said substrate and said first layer are separated by a Si-Ge interlayer.